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Presenters

Jim Bruister

President SoC Solutions

Errett Hogrefe

Senior Development Manager

- **Why SPI ? …**

or 

  - We will discuss why Serial Flash chips are used in many products. What are the advantages and some of the disadvantages.

  - We will explore how SoC Solutions' SPI and QSPI IP Cores can be used with SPI / QSPI Flash Memories in microprocessor based SOCs and systems.

About Us…

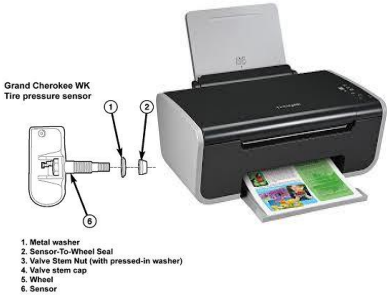
- System on Chip (SOC) Silicon IP and Integration Company
- Based in Georgia, USA – Incorporated in 2000
- Specializing in AMBA® based AXI and AHB Subsystems
  - Targeting the IoT, M2M and low power/performance device markets
- Thorough knowledge of ARM Cortex-M0, M3, A5, Dual A9 as well as similar processors from other CPU vendors.
- Developed ARM based SOCs for over 25 years
  - 1st ARM design was with VLSI Technology in 1988

Why Flash ?

- Microprocessor based SOCs need Flash
  - On-chip Flash is expensive or un-available in the process technology
  - On-chip SRAM is volatile and expensive
  - Often need larger memory for program images
  - Non-volatile Boot source
  - Need Flash Loader program / methodology

- Why Serial Flash… ***or Why SPI ?***

SPI Flash Enabled Products

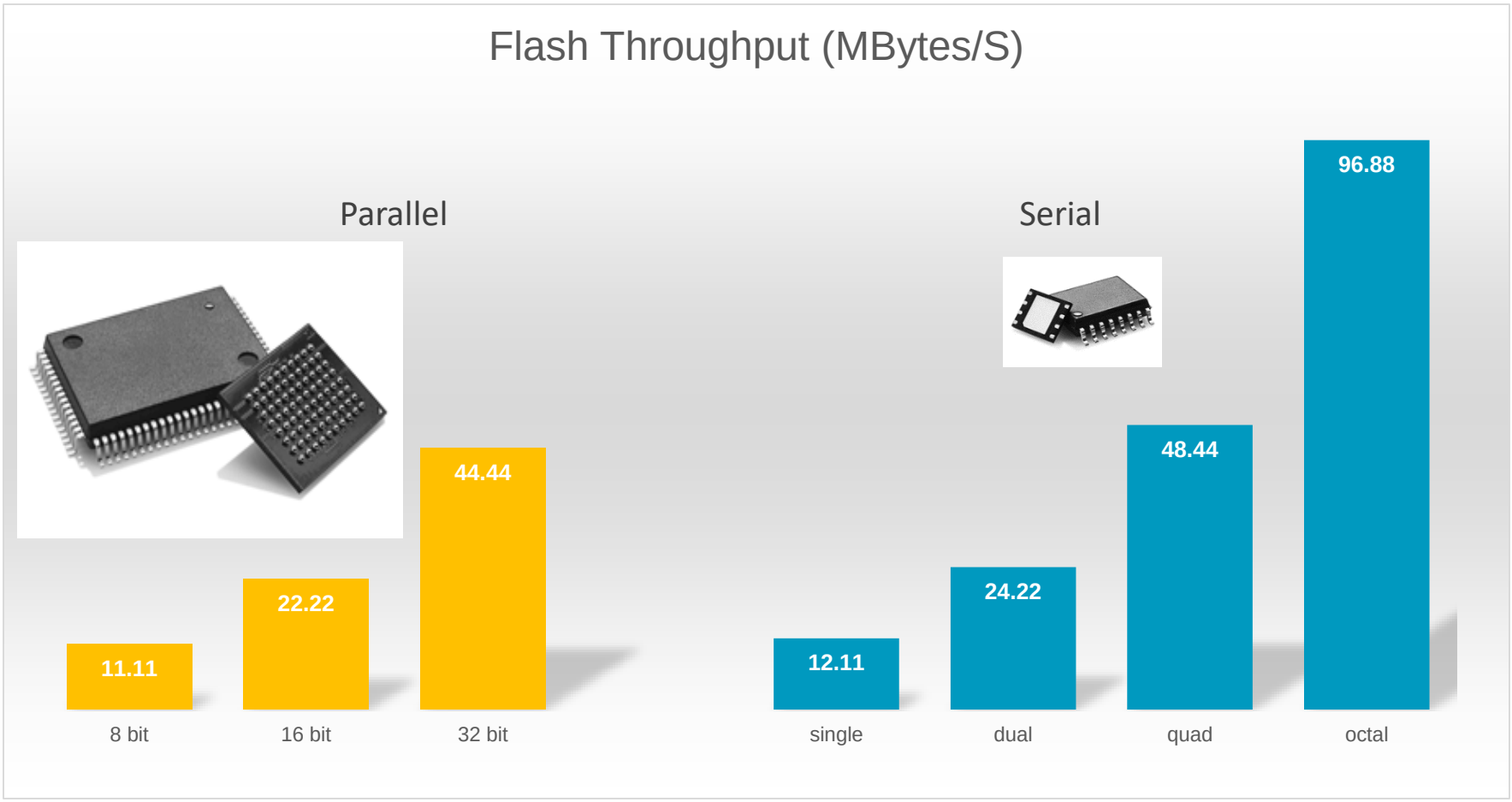


(a) (b)

Serial Flash Advantages

- Fewer Pins
  - Easy to use
  - Lower power
- Scalability
  - Wide range of Memory Densities
  - Common footprints allow upgrades without PCB re-layout
- Less Expensive Product Cost
  - Reduced PCB real estate
  - Smaller devices. Simpler routing
- Faster acquisition with Dual, Quad and Octal modes
  - Quad and Octal devices balance good performance with power efficiency
  - Clock rates are now typically > 100Mhz.

Serial Flash Advantages



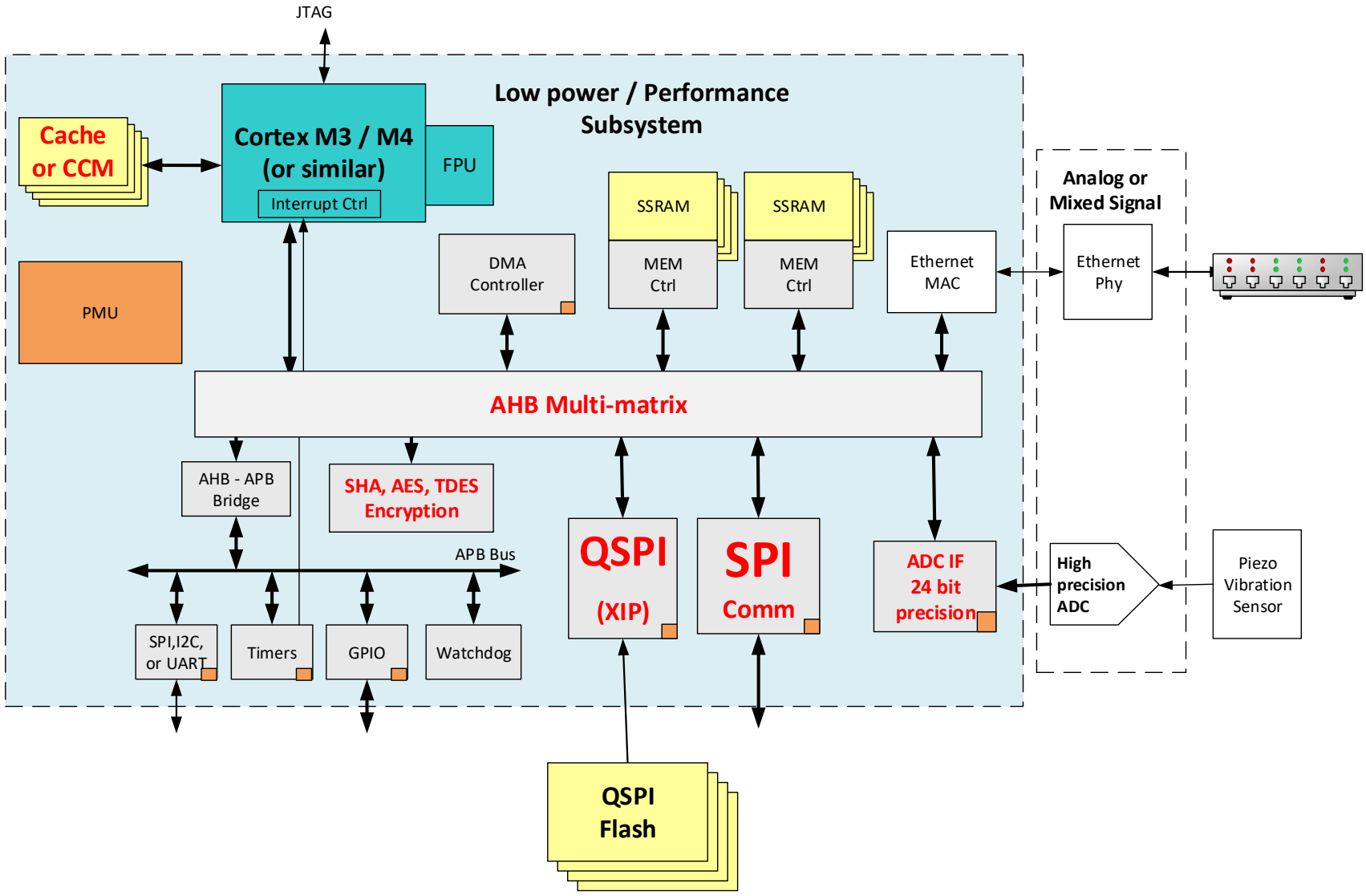
* Based on 90ns access time

* Based on 80Mhz serial clock rate

Serial Flash Disadvantages

- Smaller Memory sizes compared to Parallel Flash
- Programming time is typically longer
  - However, serial Flash has smaller sectors
- Needs a SPI protocol to read or program
  - Often done in software
  - Requires 2 serial transactions in order to read data word
    - Address word + data word
- Sometimes requires mode changes between functions
  - Such as reading the ID versus reading Quad Data

Typical IoT Chip



SOC Advantages using QSPI

- Lower Power
  - 4 to 8 IO compared to > 32 for parallel flash
- Large Non-volatile memory source
  - Up to 512M compared to very limited on chip flash
- Reduced ASIC / SOC IC cost
  - Fewer bond pads = smaller die
  - Cheaper packages
  - Reduced assembly cost
- Smaller package footprint
  - Good for small embedded products, SIPs or modules

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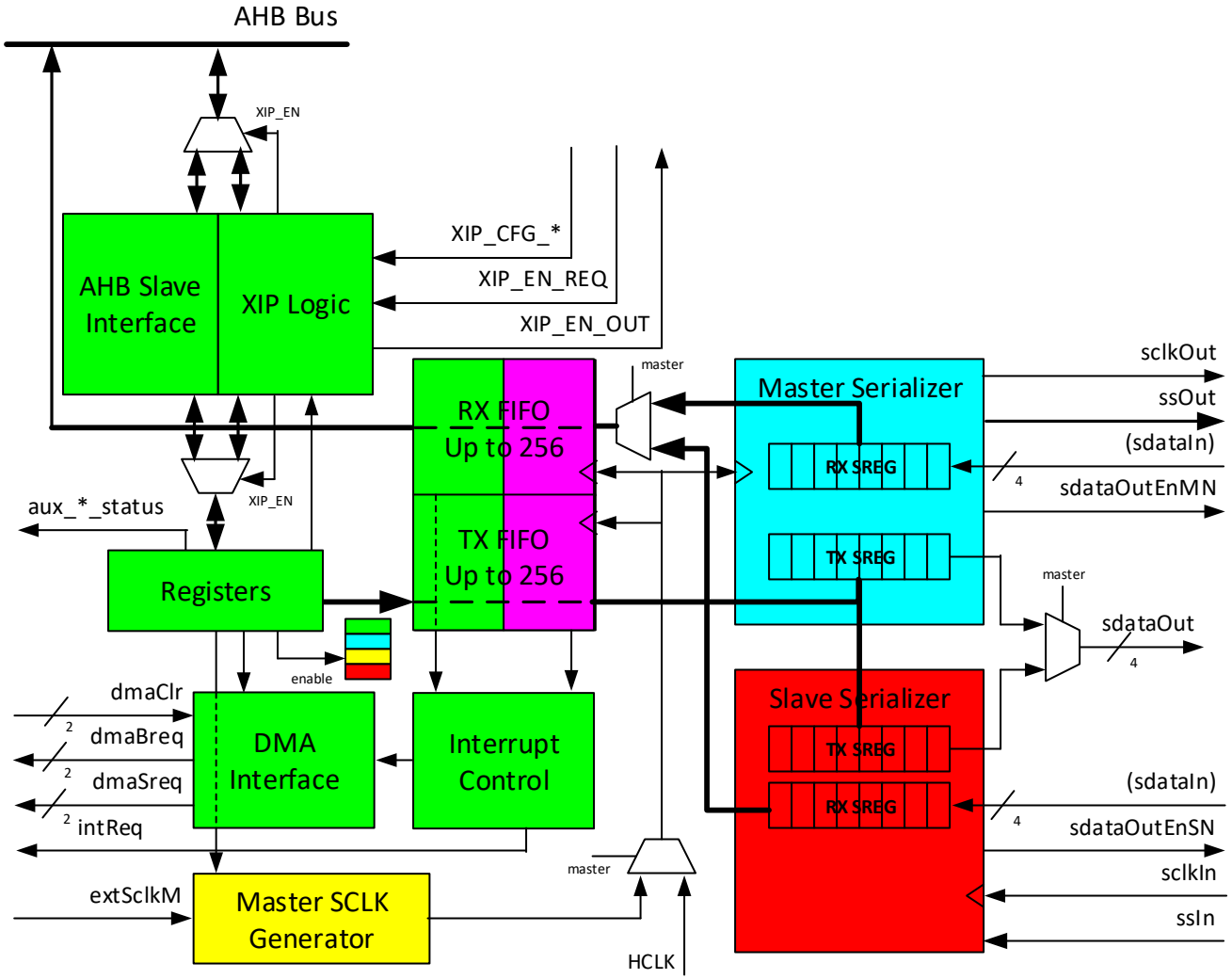
QSPI *Solutions*

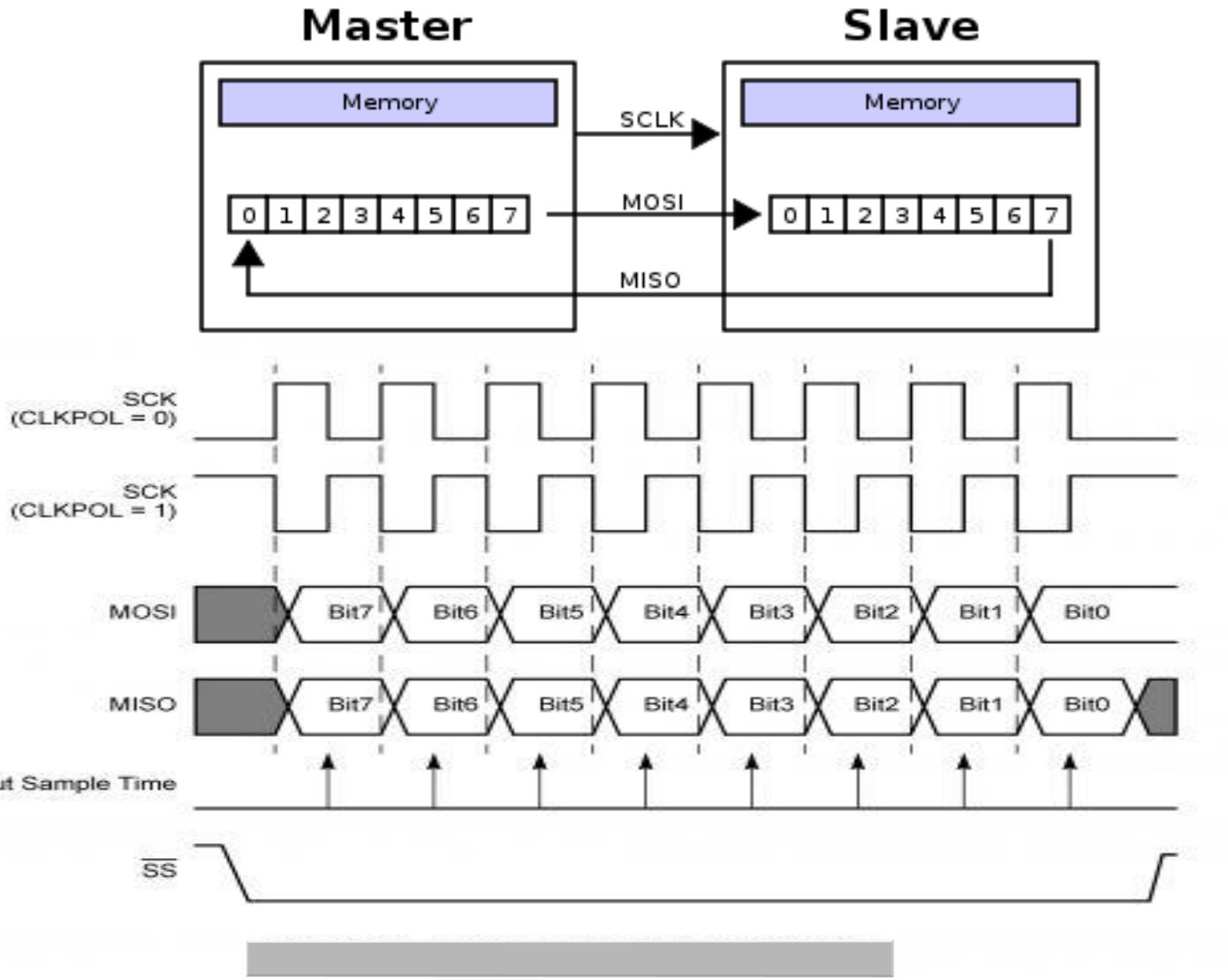
QSPI IP Core


AHB Bus
XIP_EN
AHB Slave Interface
XIP Logic
XIP_CFG_*
XIP_EN_REQ
XIP_EN_OUT
RX FIFO Up to 256
TX FIFO Up to 256
master
Master Serializer
RX SREG
TX SREG
sclkOut
ssOut
(sdataIn)
4
sdataOutEnMN
XIP_EN
aux_*_status
Registers
enable
master
sdataOut
4
dmaClr
2
dmaBreq
2
dmaSreq
2
intReq
DMA Interface
Interrupt Control
Slave Serializer
TX SREG
RX SREG
(sdataIn)
4
sdataOutEnSN
sclkIn
ssIn
extSclkM
Master SCLK Generator
master
HCLK

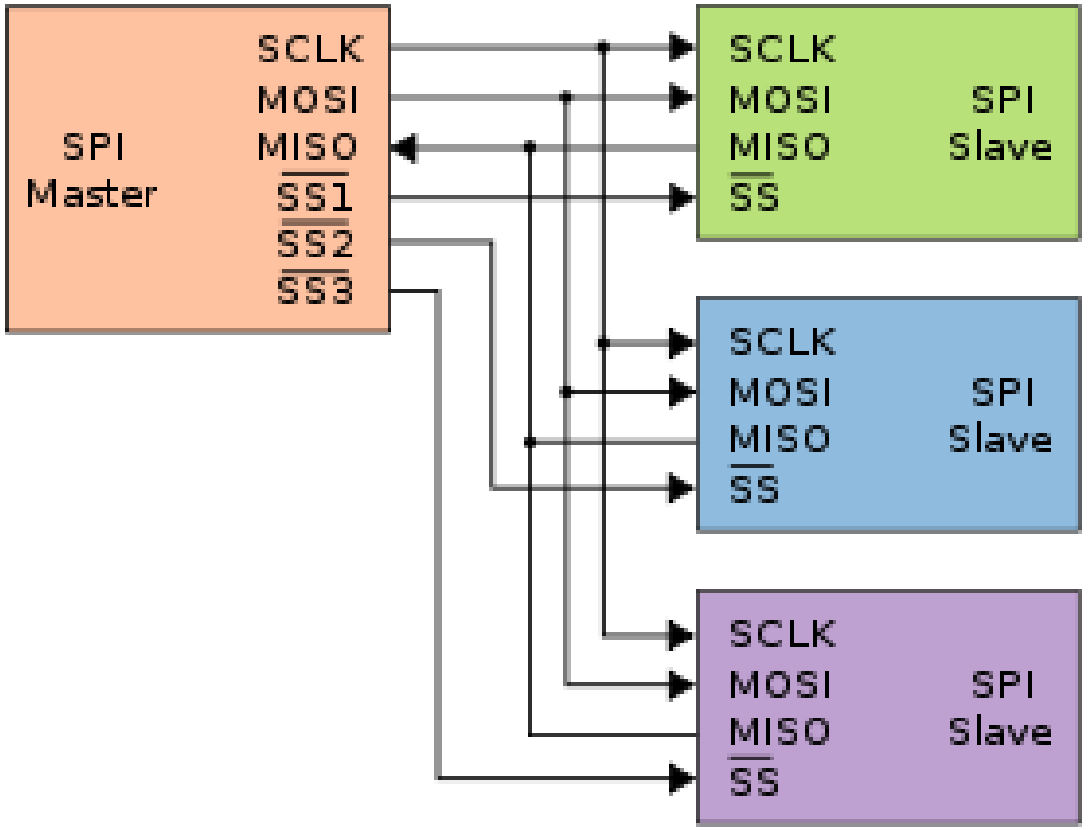
QSPI Features

- Features:
  - AMBA® AHB interface
  - Execute-in-place (XIP) functionality for industry-standard Flash device
  - 4 bit to 32 bit serial transmit & receive
  - Software programmable Master or Slave mode
  - Software programmable Master SCLK rate
  - Quad, Dual and Single-bit mode operation
  - Configurable Transmit and Receive FIFOs (up to 256 words)
  - Up to 4 slaves under Master control
  - DMA interface
  - More…

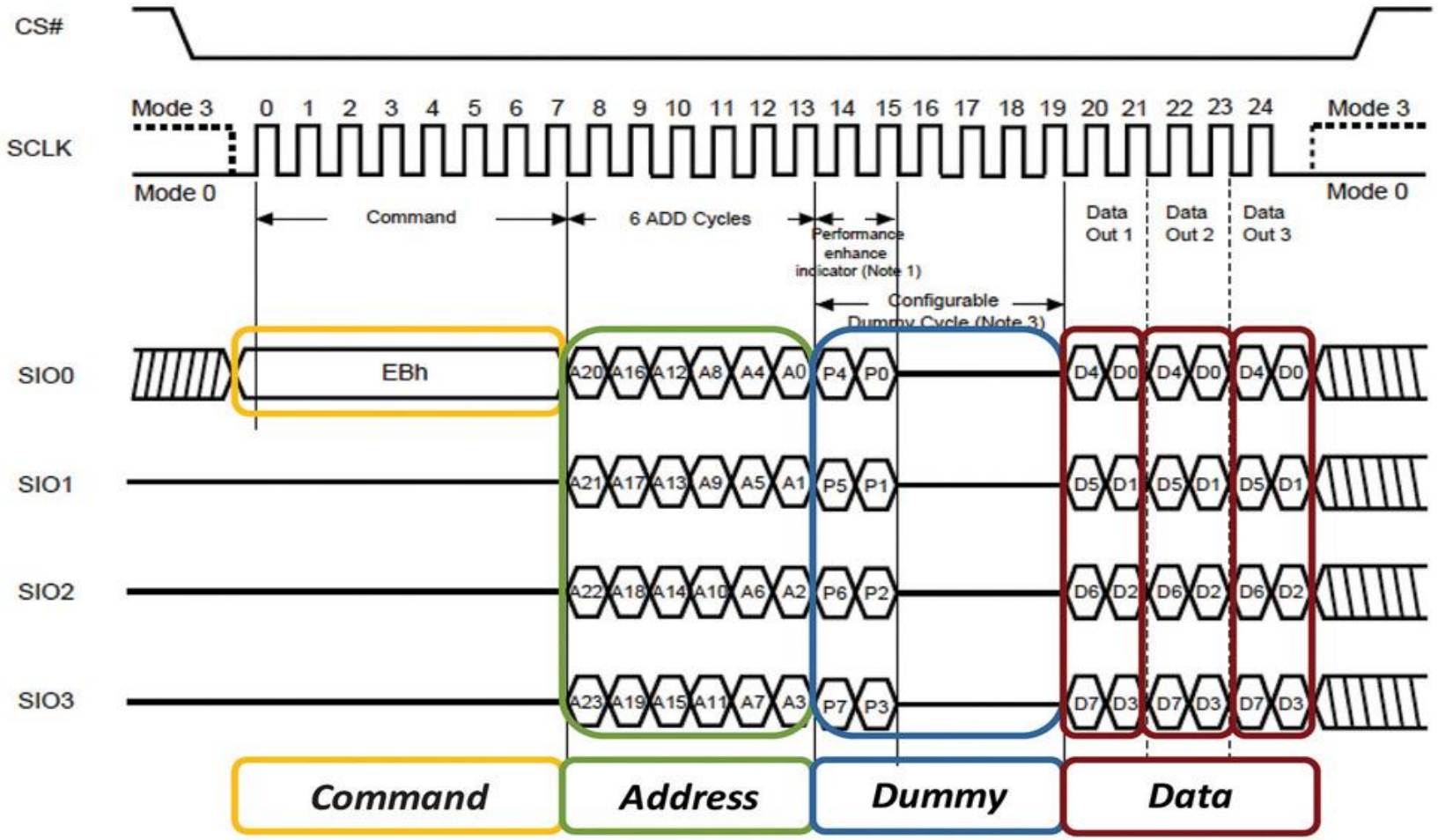
General Functionality



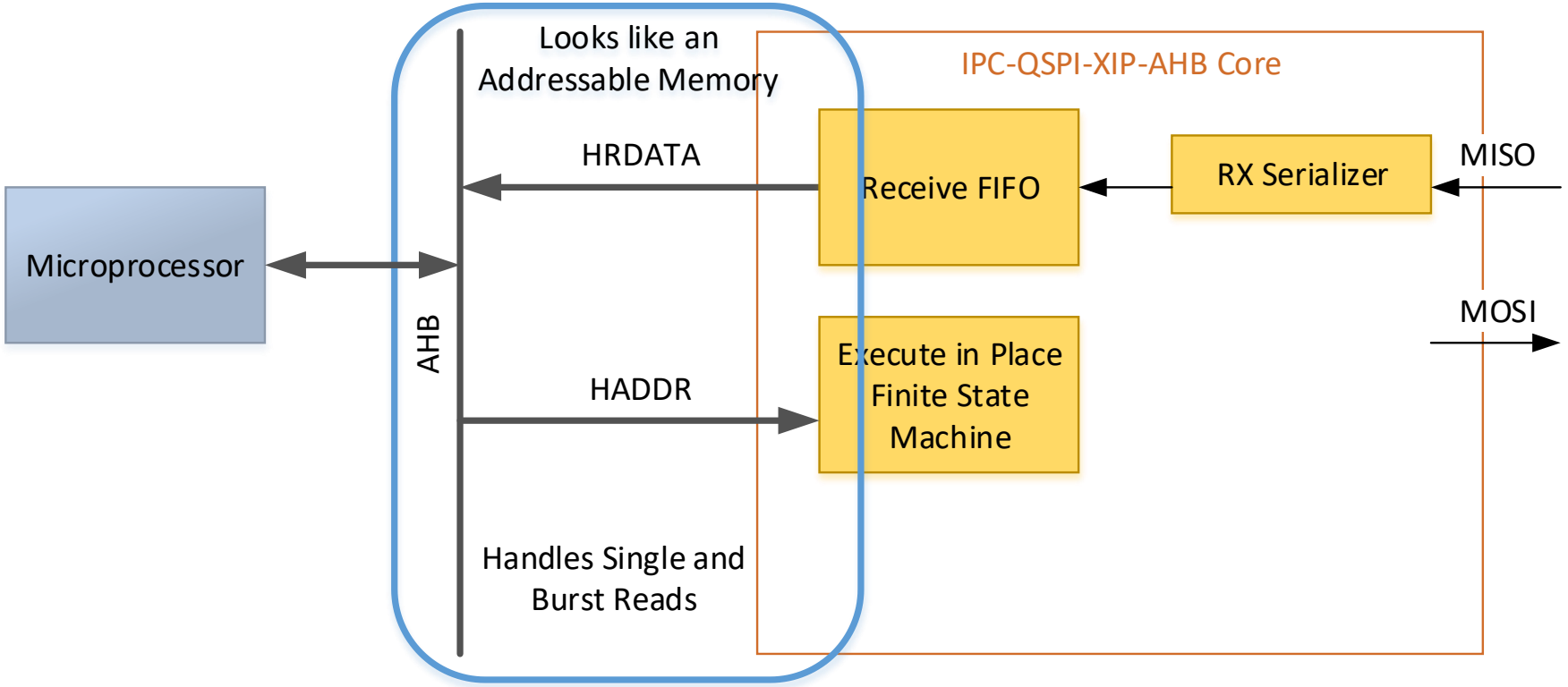
General Functionality



QUAD Transaction



Execute In Place (XIP)



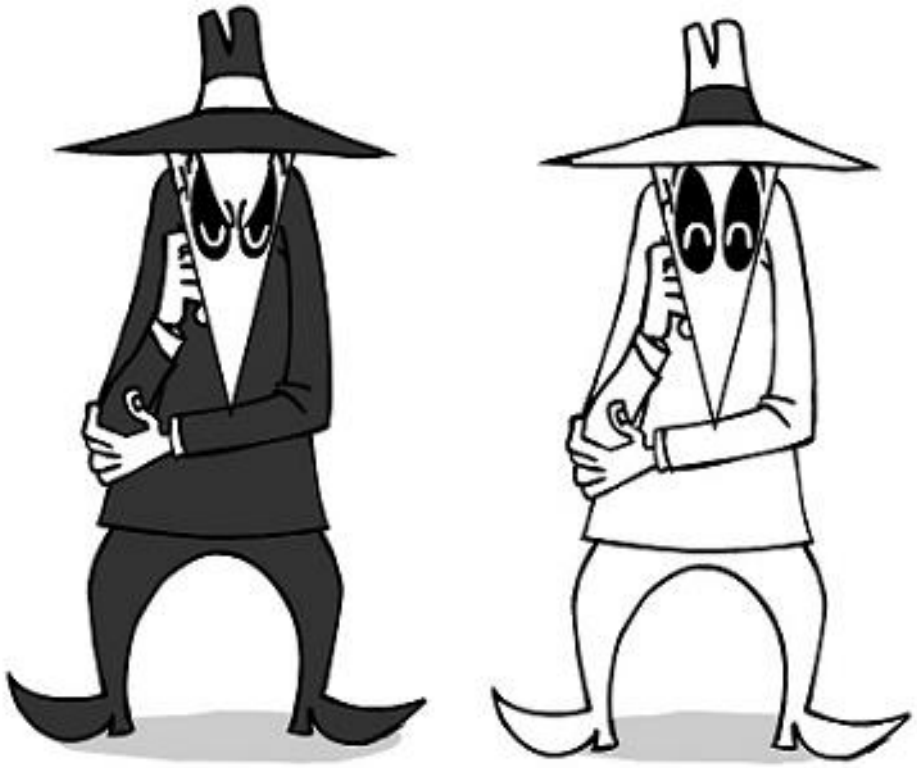
Execute In Place (XIP)

- Allows AHB Master to directly read contents from industry-standard Serial Flash devices.
  - Winbond, Macronix, Spansion, and Micron
- XIP Finite State Machine:
  - Converts AHB read transactions to SPI protocol and transactions needed to read data from Serial Flash.
- Data "Look-ahead" (pseudo cache)
  - Reads data in 32bit chucks and continues until the Rx FIFO is half full.
  - If transaction is a burst access then the next FIFO data is read.
  - If transaction is a non-sequential or single access then the FIFO is flushed after the read.

Software Support

- QSPI Boot Loader
  - *Copies Flash image to internal SRAM then re-boots*
  - Out of the box for Cortex-M0/M3
  - Mostly C-Code with small amount of Assembly
  - Examples for other processors
- QSPI Flash Loader
  - *Writes an image to external Serial Flash*
  - The image is loaded via JTAG or UART to internal SRAM then paged to Flash
  - Handles paging the image

What's next ?



It’s here already !!!

- AXI QSPI
  - Configurable 32 or 64 bit
- AHB Octal SPI with DTR
  - 8 serial channels to support the industry-standard Octal Flash Parts
  - Double Transfer Rate (DTR) *2x throughput*
  - Micron, Macronix, Spansion and Winbond

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Questions ?