

FEATURES

- Translates AMBA® AHB transactions to APB transactions
- Low latency
- Low Gate Count
- Supports APB 2.0 and APB 3.0 Signaling
- Independent HCLK, PCLK pseudo-synchronous clocks

LICENSED IP PACKAGE INCLUDES

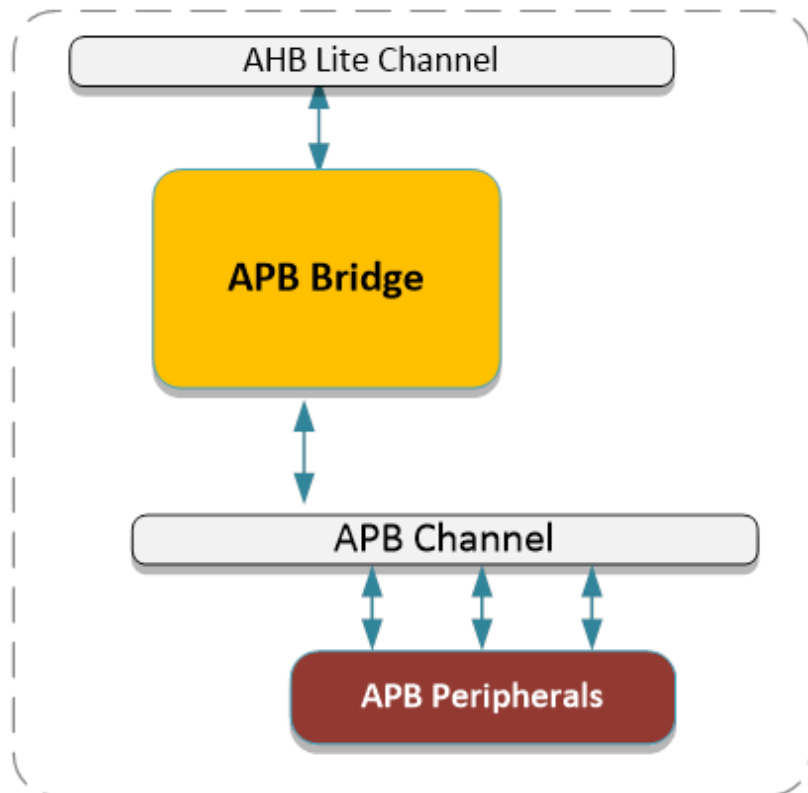
- Verilog Source
- Complete Test Environment
- AHB Bus Functional Model
- C-Sample Code

DESCRIPTION

The AHB to APB Bridge translates an AHB bus transaction (read or write) to an APB bus transaction. This is accomplished via two small state machines - one on the HCLK domain and another on the PCLK domain.

The AHB to APB Bridge acts as an AHB Slave, and an APB Master in an AHB/APB subsystem. Typically, the AHB to APB Bridge has its AHB interface connected to a Slave port on an AHB Channel module, and its APB interface connected to the Master port on an APB Channel module.

GENERAL USE



You may also be interested in:

AMBA® Subsystems

- Low Power Subsystem (simple AHB system)
- Low Power / Performance Subsystem (includes AHB Multi-matrix Fabric)
- Custom Performance Subsystem (includes AXI Multi-layer Fabric)

IP Cores

Infrastructure Cores

AHB Multi-Matrix Fabric
AHB/AHBLite Channel
AHB Arbiter
AXI Multi-Layer Fabric
AXI to AHBLite Bridge
AXI to APB Bridge
AHB to ABP Bridge
APB Channel

AXI Cores

AXI Multi-Layer Fabric
AXI to AHBLite Bridge
AXI to APB Bridge
AXI External Bus Interface
(Memory/Flash Controller)
AXI Internal Memory Controller
AXI QSPI with Execute in Place (XIP)

AHB Cores

AHB Channel
AHB Multi-Matrix Fabric
AHB to ABP Bridge
AHB Arbiter
AHB QSPI with Execute in Place (XIP)
AHB External Bus Interface
AHB Internal SRAM Controller
AHB Interrupt Controller
AHB DMA Controller
AHB DMA 4 Channel Controller
AHB TFT LCD Controller
AHB DES/TDES Encryption/Decryption

AHB Serial Flash Controller
Octal, Quad, Dual and Single Modes

Serial to AHB Bridge
SPI slave to AHB Master
Monitor/Control

APB Cores

APB Channel
APB Quad SPI Controller
APB General Purpose IO
APB Timer
APB UART
APB I2C (Master and Slave)
APB SPI
APB Watchdog Timer
APB Pulse Width Modulator
APB Real Time Clock

General

DES – Digital Encryption Standard
Triple DES (Low Gates)
Triple DES (pipelined)
ADC Interface (semi-custom)
Mixed-Signal Interfaces (semi-custom)
Power Management Unit (semi-custom)

AES Encryption Core

For more information contact



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