AXI - APB Bridge

IP Core

IPC-ApbBridge-AXI

FEATURES

- Translates AMBA® AXI transactions to APB transactions
- Low latency
- Low Gate Count
- Supports APB 2.0 and APB 3.0 Signaling
- Independent ACLK, PCLK pseudo-synchronous clocks

LICENSED IP PACKAGE INCLUDES

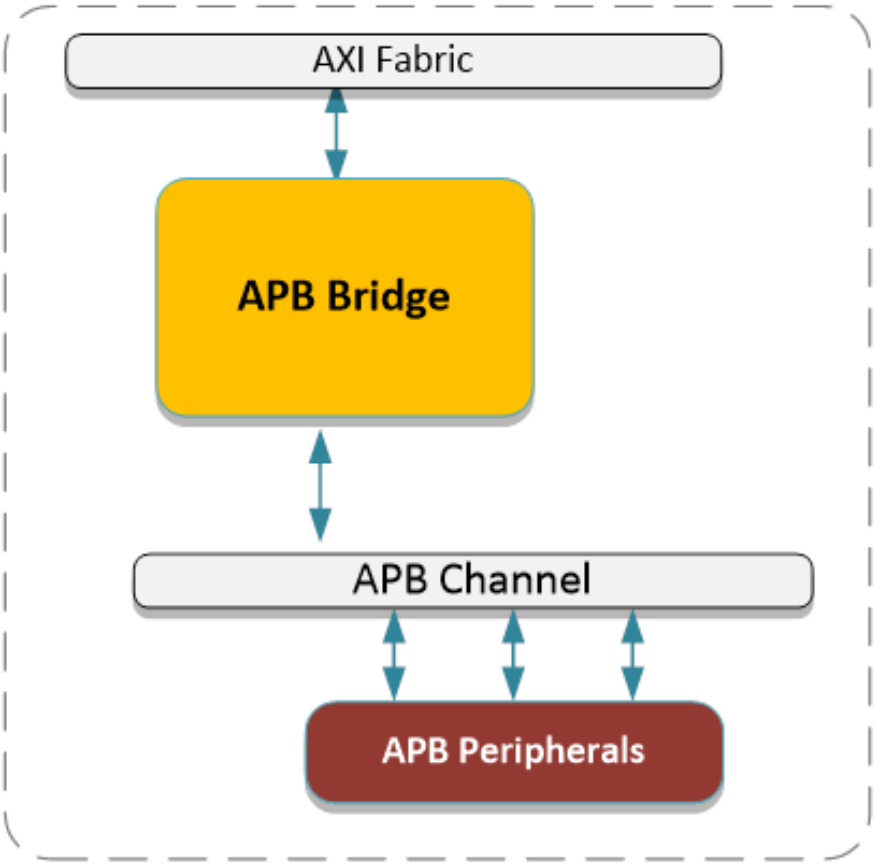
- Verilog Source
- Complete Test Environment
- AXI Bus Functional Model

DESCRIPTION

The AXI to APB Bridge translates an AXI bus transaction (read or write) to an APB bus transaction. This is accomplished via two state machines – one governing the AXI transactions, and one governing APB transactions.

The AXI to APB Bridge acts as an AXI Slave, and an APB Master in an AXI/APB subsystem. Typically, the AXI to APB Bridge has its AXI interface connected to a Slave port on an AXI Channel/Interconnect module, and its APB interface connected to the Master port on an APB Channel module.

GENERAL USE



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You may also be interested in:

AMBA® Subsystems

- Low Power Subsystem (simple AHB system)
- Low Power / Performance Subsystem (includes AHB Multi-matrix Fabric)
- Custom Performance Subsystem (includes AXI Multi-layer Fabric)

IP Cores

Infrastructure Cores

AHB Multi-Matrix Fabric
AHB/AHBLite Channel
AHB Arbiter
AXI Multi-Layer Fabric
AXI to AHBLite Bridge
AXI to APB Bridge
AHB to ABP Bridge
APB Channel

AXI Cores

AXI Multi-Layer Fabric
AXI to AHBLite Bridge
AXI to APB Bridge
AXI External Bus Interface
(Memory/Flash Controller)
AXI Internal Memory Controller
AXI QSPI with Execute in Place (XIP)

AHB Cores

AHB Channel
AHB Multi-Matrix Fabric
AHB to ABP Bridge
AHB Arbiter
AHB QSPI with Execute in Place (XIP)
AHB External Bus Interface
AHB Internal SRAM Controller
AHB Interrupt Controller
AHB DMA Controller
AHB DMA 4 Channel Controller
AHB TFT LCD Controller
AHB DES/TDES Encryption/Decryption

AHB Serial Flash Controller
Octal, Quad, Dual and Single Modes

Serial to AHB Bridge
SPI slave to AHB Master
Monitor/Control

APB Cores

APB Channel
APB Quad SPI Controller
APB General Purpose IO
APB Timer
APB UART
APB I2C (Master and Slave)
APB SPI
APB Watchdog Timer
APB Pulse Width Modulator
APB Real Time Clock

General

DES – Digital Encryption Standard
Triple DES (Low Gates)
Triple DES (pipelined)
ADC Interface (semi-custom)
Mixed-Signal Interfaces (semi-custom)
Power Management Unit (semi-custom)

AES Encryption Core

For more information contact

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