AHB Lite to AXI Bridge

IP Core

IPC-AxiBridge-AHB

FEATURES

- Converts AHBLite Master transactions to AXI Master transactions
- Pseudo-synchronous clock domains
- FIFOs for Buffering

LICENSED IP PACKAGE INCLUDES

- Verilog Source
- Complete Test Environment
- AHB Bus Functional Model

DESCRIPTION

The AHB Lite to AXI Bridge translates an AHB Lite bus transaction (read or write) to an AXI bus transaction. It is expected that the AXI clock and the AHB clock are derived from the same clock source, and that the period of the AHB Lite clock is an integer multiple of the AXI clock in the range [1,16].

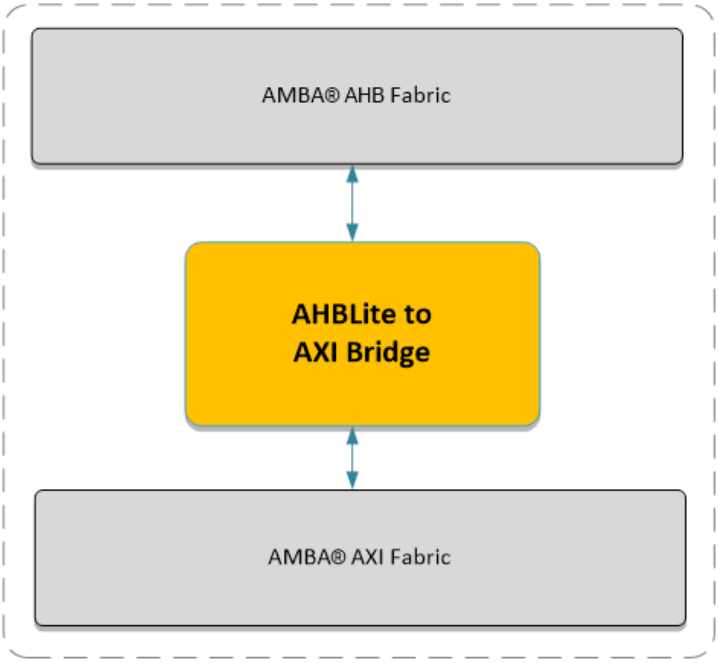
Logic on two synchronous clock domains is used to accomplish the translation.

The AHB Lite logic is responsible for responding to transaction requests from the AHB Lite, and for generating AXI transactions based on transaction information from the AHB logic, and for presenting read data from the AXI subsystem back to the AHB Lite Master.

The AXI logic is responsible for generating AXI transactions based on transaction information from the AHB Lite logic, and for pacing the AXI transaction based on internal FIFO levels and on responses from the AXI Slave peripheral.

The AHB Lite to AXI Bridge acts as an AHB Lite Slave, and an AXI Master in an AXI/AHB subsystem. Typically, the AHB Lite to AXI Bridge has its AHB Lite interface connected to a Slave port on an AHB Lite Channel/Interconnect module, and its AXI interface connected to the Master port on an AXI Channel module.

GENERAL USE



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You may also be interested in:

AMBA® Subsystems

- Low Power Subsystem (simple AHB system)
- Low Power / Performance Subsystem (includes AHB Multi-matrix Fabric)
- Custom Performance Subsystem (includes AXI Multi-layer Fabric)

IP Cores

Infrastructure Cores

AHB Multi-Matrix Fabric
AHB/AHBLite Channel
AHB Arbiter
AXI Multi-Layer Fabric
AXI to AHBLite Bridge
AXI to APB Bridge
AHB to ABP Bridge
APB Channel

AXI Cores

AXI Multi-Layer Fabric
AXI to AHBLite Bridge
AXI to APB Bridge
AXI External Bus Interface
(Memory/Flash Controller)
AXI Internal Memory Controller
AXI QSPI with Execute in Place (XIP)

AHB Cores

AHB Channel
AHB Multi-Matrix Fabric
AHB to ABP Bridge
AHB Arbiter
AHB QSPI with Execute in Place (XIP)
AHB External Bus Interface
AHB Internal SRAM Controller
AHB Interrupt Controller
AHB DMA Controller
AHB DMA 4 Channel Controller
AHB TFT LCD Controller
AHB DES/TDES Encryption/Decryption

AHB Serial Flash Controller
Octal, Quad, Dual and Single Modes

Serial to AHB Bridge
SPI slave to AHB Master
Monitor/Control

APB Cores

APB Channel
APB Quad SPI Controller
APB General Purpose IO
APB Timer
APB UART
APB I2C (Master and Slave)
APB SPI
APB Watchdog Timer
APB Pulse Width Modulator
APB Real Time Clock

General

DES – Digital Encryption Standard
Triple DES (Low Gates)
Triple DES (pipelined)
ADC Interface (semi-custom)
Mixed-Signal Interfaces (semi-custom)
Power Management Unit (semi-custom)

AES Encryption Core

For more information contact

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