DMA-4 Controller

IP Core

IPC-DMA4-AHB

FEATURES

- AMBA® AHB Master/Slave DMA Controller
- Four DMA Channels
- Internal Arbitration for Single AHB Master Interface
- Memory to Memory. Memory to Peripheral, Peripheral to Memory, Peripheral to Peripheral modes
- Source and destination address descriptors
- Single word and burst transfer requests
- Programmable burst size
- Current address status
- Incrementing and non-incrementing addressing
- Linked list support
- Transfer complete interrupt

LICENSED IP PACKAGE INCLUDES

- Verilog Source
- Complete Test Environment
- AHB Bus Functional Model

DESCRIPTION

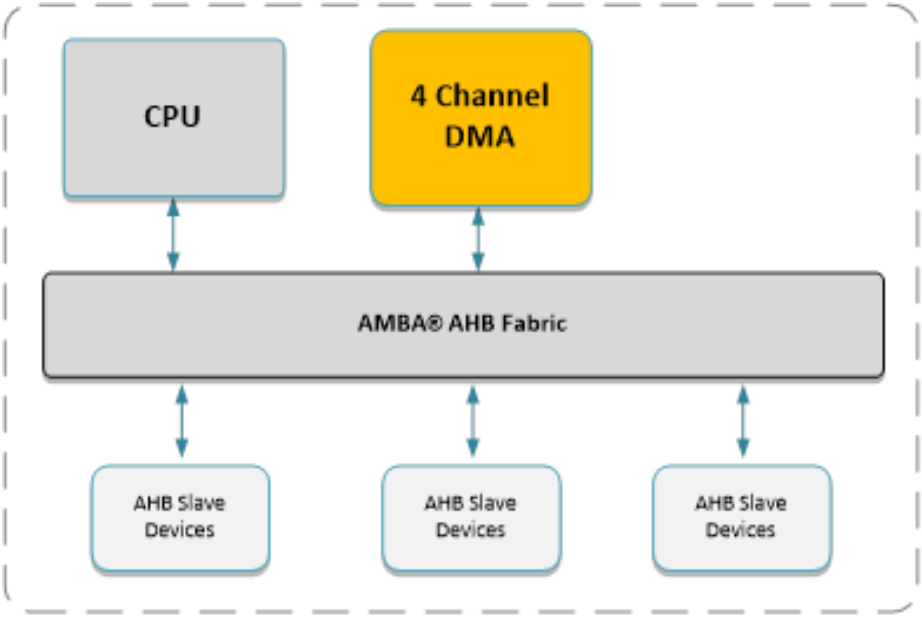
The DMA is a multiple-channel direct memory access controller. The DMA IP Core is a Verilog HDL design that can be used in ASIC, Structured ASIC and FPGA designs. The design is intended to be used with AMBA based systems as a controller to transfer data directly from system memory to memory or system memory to peripheral device or IP Core.

Once configured and enabled, the DMA controller is primarily an AHB Master, which initiates data transfers across the AHB bus to/from a peripheral device through the DMA Buffer. The DMA Buffer is a 16x32bit FIFO, which is useful for peripheral devices requiring a steady stream of data such as an LCD Controller, Ethernet MAC or other communication device.

The DMA controller contains useful features such incrementing and non-incrementing addressing and link list operation. Linked list support is useful for non-contiguous memory transfer operations.

The DMA Channel Arbiter determines which DMA Channel has access to the external AHB Master Bus. A round-robin algorithm is implemented in which each active channel has equal priority.

GENERAL USE



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You may also be interested in:

AMBA® Subsystems

- Low Power Subsystem (simple AHB system)
- Low Power / Performance Subsystem (includes AHB Multi-matrix Fabric)
- Custom Performance Subsystem (includes AXI Multi-layer Fabric)

IP Cores

Infrastructure Cores

AHB Multi-Matrix Fabric
AHB/AHBLite Channel
AHB Arbiter
AXI Multi-Layer Fabric
AXI to AHBLite Bridge
AXI to APB Bridge
AHB to ABP Bridge
APB Channel

AXI Cores

AXI Multi-Layer Fabric
AXI to AHBLite Bridge
AXI to APB Bridge
AXI External Bus Interface
(Memory/Flash Controller)
AXI Internal Memory Controller
AXI QSPI with Execute in Place (XIP)

AHB Cores

AHB Channel
AHB Multi-Matrix Fabric
AHB to ABP Bridge
AHB Arbiter
AHB QSPI with Execute in Place (XIP)
AHB External Bus Interface
AHB Internal SRAM Controller
AHB Interrupt Controller
AHB DMA Controller
AHB DMA 4 Channel Controller
AHB TFT LCD Controller
AHB DES/TDES Encryption/Decryption

AHB Serial Flash Controller
Octal, Quad, Dual and Single Modes

Serial to AHB Bridge
SPI slave to AHB Master
Monitor/Control

APB Cores

APB Channel
APB Quad SPI Controller
APB General Purpose IO
APB Timer
APB UART
APB I2C (Master and Slave)
APB SPI
APB Watchdog Timer
APB Pulse Width Modulator
APB Real Time Clock

General

DES – Digital Encryption Standard
Triple DES (Low Gates)
Triple DES (pipelined)
ADC Interface (semi-custom)
Mixed-Signal Interfaces (semi-custom)
Power Management Unit (semi-custom)

AES Encryption Core

For more information contact

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