I2C Slave
IP Core
IPC-12CSlave-APB

FEATURES

- AMBA® APB Compatible
- Standard I2C - Inter-Integrated Circuit Bus Interface
- I2C Slave Mode
- I2C Transmit and Receive Engine
- AMBA® APB Configuration Registers
- Read and Write FIFOs
- Interrupt Generation Logic

LICENSED IP PACKAGE INCLUDES

- Verilog Source
- Complete Test Environment
- AHB Bus Functional Model
- C-Sample Code

DESCRIPTION

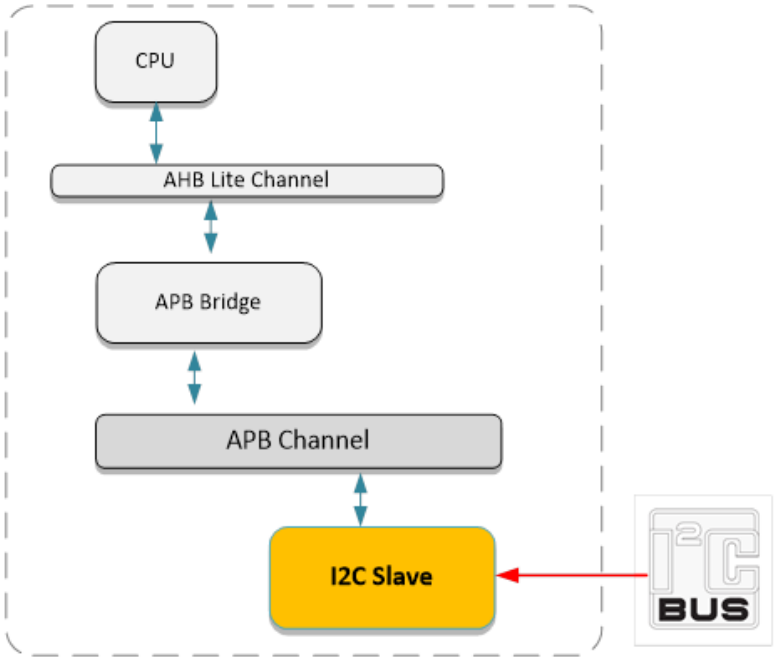
This is an implementation of an I2C Slave with a FIFO interface to the AMBA APB bus. The I2C peripheral contains the following main sections:

- Configuration Registers
- Read and Write FIFOs
- Interrupt Generator
- I2C Engine

Configuration registers are written and read by the processor via an APB Interface.

The I2C engine converts I2C read/write requests into FIFO writes/reads. I2C writes usually occur with no delay; however, reads usually cause the engine to assert SCL low (stretch the clock) to gain time for the read request to be fulfilled by the processor through the APB. An interrupt is generated to facilitate this. If the processor keeps the FIFOs full this overhead can be minimized. Optionally, a flow control mode may be selected which stretches the clock for all reads and writes. In this mode the processor must respond to an interrupt and clear the stretching.

GENERAL USE



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You may also be interested in:

AMBA® Subsystems

- Low Power Subsystem (simple AHB system)
- Low Power / Performance Subsystem (includes AHB Multi-matrix Fabric)
- Custom Performance Subsystem (includes AXI Multi-layer Fabric)

IP Cores

Infrastructure Cores

AHB Multi-Matrix Fabric
AHB/AHBLite Channel
AHB Arbiter
AXI Multi-Layer Fabric
AXI to AHBLite Bridge
AXI to APB Bridge
AHB to ABP Bridge
APB Channel

AXI Cores

AXI Multi-Layer Fabric
AXI to AHBLite Bridge
AXI to APB Bridge
AXI External Bus Interface
(Memory/Flash Controller)
AXI Internal Memory Controller
AXI QSPI with Execute in Place (XIP)

AHB Cores

AHB Channel
AHB Multi-Matrix Fabric
AHB to ABP Bridge
AHB Arbiter
AHB QSPI with Execute in Place (XIP)
AHB External Bus Interface
AHB Internal SRAM Controller
AHB Interrupt Controller
AHB DMA Controller
AHB DMA 4 Channel Controller
AHB TFT LCD Controller
AHB DES/TDES Encryption/Decryption

AHB Serial Flash Controller
Octal, Quad, Dual and Single Modes

Serial to AHB Bridge
SPI slave to AHB Master
Monitor/Control

APB Cores

APB Channel
APB Quad SPI Controller
APB General Purpose IO
APB Timer
APB UART
APB I2C (Master and Slave)
APB SPI
APB Watchdog Timer
APB Pulse Width Modulator
APB Real Time Clock

General

DES – Digital Encryption Standard
Triple DES (Low Gates)
Triple DES (pipelined)
ADC Interface (semi-custom)
Mixed-Signal Interfaces (semi-custom)
Power Management Unit (semi-custom)

AES Encryption Core

For more information contact

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