SPI-AHBLite Bridge
IP Core
IPC-SpiAhbLiteBridge-AHB

FEATURES

- AMBA® AHB Monitor
- Allows external devices to access the internal AHB Bus
- AHB Master Read/Write capability
- Useful for updating device software from and external device
- Useful for reading internal memory mapped registers and memory

LICENSED IP PACKAGE INCLUDES

- Verilog Source
- Complete Test Environment
- AHB Bus Functional Model
- C-Sample Code

DESCRIPTION

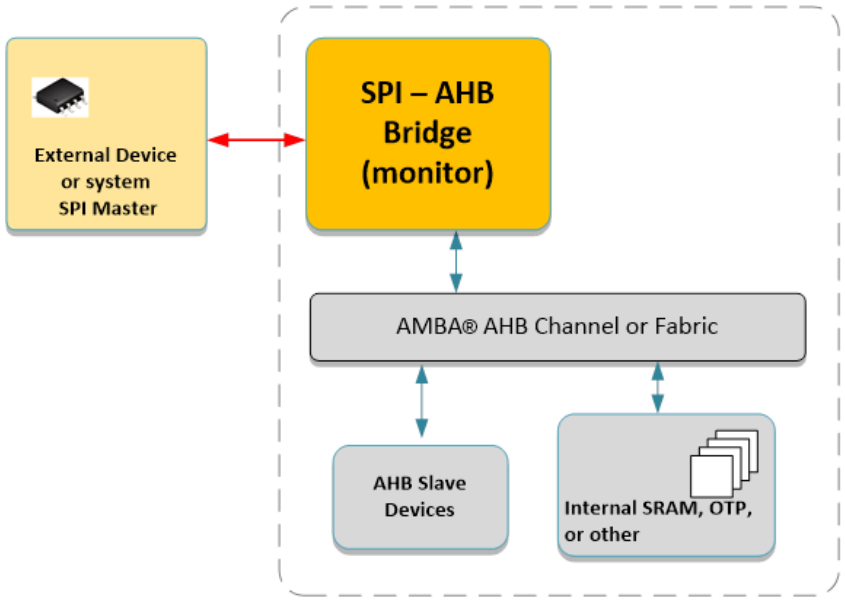
The IPC-SpiAhbLiteBridge-AHB IP core is commonly used as a monitor interface to allow external devices to access the internal AHB bus.

A SPI Slave to AHB Lite Interface block (socSpiAhbLiteBridge) provides read/write access by an external SPI device to the various memories and registers that are present in the chip's internal AHB Lite subsystem. The Bridge converts SPI transactions into AHB Read or Write instructions, allowing the external SPI device to have full access to all memory mapped devices present in the AHB Lite subsystem.

The SPI protocol layer is responsible for several things including:

- Interpreting commands from the low-level SPI interface (R/W, address, mode, protection, burst length).
- Generating an AHB Read or Write transaction based on the command received from the SPI interface.
- Presenting (parallel) address and write data from the low-level SPI interface to the system.
- Presenting (parallel) read data from the system to the low-level SPI interface.

GENERAL USE



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You may also be interested in:

AMBA® Subsystems

- Low Power Subsystem (simple AHB system)
- Low Power / Performance Subsystem (includes AHB Multi-matrix Fabric)
- Custom Performance Subsystem (includes AXI Multi-layer Fabric)

IP Cores

Infrastructure Cores

AHB Multi-Matrix Fabric
AHB/AHBLite Channel
AHB Arbiter
AXI Multi-Layer Fabric
AXI to AHBLite Bridge
AXI to APB Bridge
AHB to ABP Bridge
APB Channel

AXI Cores

AXI Multi-Layer Fabric
AXI to AHBLite Bridge
AXI to APB Bridge
AXI External Bus Interface
(Memory/Flash Controller)
AXI Internal Memory Controller
AXI QSPI with Execute in Place (XIP)

AHB Cores

AHB Channel
AHB Multi-Matrix Fabric
AHB to ABP Bridge
AHB Arbiter
AHB QSPI with Execute in Place (XIP)
AHB External Bus Interface
AHB Internal SRAM Controller
AHB Interrupt Controller
AHB DMA Controller
AHB DMA 4 Channel Controller
AHB TFT LCD Controller
AHB DES/TDES Encryption/Decryption

AHB Serial Flash Controller
Octal, Quad, Dual and Single Modes

Serial to AHB Bridge
SPI slave to AHB Master
Monitor/Control

APB Cores

APB Channel
APB Quad SPI Controller
APB General Purpose IO
APB Timer
APB UART
APB I2C (Master and Slave)
APB SPI
APB Watchdog Timer
APB Pulse Width Modulator
APB Real Time Clock

General

DES – Digital Encryption Standard
Triple DES (Low Gates)
Triple DES (pipelined)
ADC Interface (semi-custom)
Mixed-Signal Interfaces (semi-custom)
Power Management Unit (semi-custom)

AES Encryption Core

For more information contact

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