Features

- AMBA® AHB Compatible
- 24 bit TFT LCD Controller.
- 32x32 Pixel FIFO.
- 256 Pixel Palette Mode.
- True Color and 24 bit Color support.
- Programmable Hsync and Vsync rates.
- Supports up to 1080p resolution (expandable)
- Pixel DMA controller.
- Programmable Interrupt Interface.
- Supports wide variety of system clock rates.

Overview

The AHB TFTLCD Controller is a configurable core that interfaces to an AHB bus and provides all the timing control and pixel serialization for controlling various TFT LCD Display Panels. The core can also be used with various RAMDACs to interface to VGA Monitors or VGA style LCD Panels.

The AHB TFTLCD Controller supports 24-bit true color and 16-bit color, as well as an 8-bit color display mode via the 256 Pixel Palette Ram. Pixel clock generation, Sync Control and Display Enable controls are fully programmable and can be used with a wide range of system clock rates.

Display information is held in system memory and is accessed by the AHB TFTLCD Controller by its internal DMA controller; DMA occurs via the AHB Master Interface. The core reads from system memory and outputs pixel information to the display. In true color mode, 24-bit pixels are accessed 32 bits at a time. In 16-bit color mode, 2 16-bit pixels are accessed 32 bits at a time and then serialized. In 8-bit color mode, 4 8-bit pixels are accessed 32 bits at a time and then serialized as 24-bit palette mapped pixels.

The LCD data interface contains 8-bit Red, 8-bit Green, and 8-bit Blue for a total of 24 bits. The LCD data interface will work with 6-bit RGB panels as well.

Interrupt sources timed to hsync, vsync and control signals are programmable and selectable to signal the processor to update display information.
The licensed IP package includes:

- Verilog Source
- Complete Verilog Test Environment
- Simulation and synthesis scripts
- C-Sample code

You may also be interested in:

- Low Power Subsystem
- Low Power / Performance Subsystem
- Custom Performance Subsystem

### Infrastructure Cores

- AHB Multi-Matrix Fabric
- AHB/AHBLite Channel
- AHB Arbiter
- AXI Multi-Layer Fabric
- AXI to AHBLite Bridge
- AXI to APB Bridge
- AHB to APB Bridge
- APB Channel

### AXI Cores

- AXI Multi-Layer Fabric
- AXI to AHBLite Bridge
- AXI to APB Bridge
- AXI External Bus Interface (Memory/Flash Controller)
- AXI Internal Memory Controller

### AHB Cores

- AHB Channel
- AHB Multi-Matrix Fabric
- AHB to APB Bridge
- AHB Arbiter
- AHB QSPI with Execute in Place (XIP)
- AHB External Bus Interface
- AHB Internal SRAM Controller
- AHB Interrupt Controller
- AHB DMA Controller
- AHB DMA 4 Channel Controller
- AHB TFT LCD Controller
- AHB DES/TDES Encryption/Decryption

### APB Cores

- APB Channel
- APB Quad SPI Controller
- APB General Purpose IO
- APB Timer
- APB UART
- APB I2C (Master and Slave)
- APB SPI
- APB Watchdog Timer
- APB Pulse Width Modulator
- APB Real Time Clock
- APB Parallel Port
- APB Remap (for boot)

### General

- DES/TDES – Digital Encryption Standard

For more information contact

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