TFT LCD Controller

IP Core

IPC-TFT-LCD

FEATURES

- 24 bit TFT LCD Controller.
- 32x32 Pixel FIFO.
- 256 Pixel Palette Mode.
- True Color and 24 bit Color support.
- Programmable Hsync and Vsync rates.
- Supports up to 2048 x 1536 resolution (expandable)
- Pixel DMA controller.
- Programmable Interrupt Interface.
- Supports wide variety of system clock rates.
- Asynchronous input clock for pixel operation.
- 8080-style parallel command/data interface

LICENSED IP PACKAGE INCLUDES

- Verilog Source
- Complete Test Environment
- AHB Bus Functional Model
- C-Sample Code

DESCRIPTION

The AHB TFTLCD Controller is a configurable core that interfaces to an AHB or generic microprocessor bus and provides all the timing control and pixel serialization for controlling various TFT LCD Display Panels. The core can also be used with various RAMDACs to interface to VGA Monitors or VGA style LCD Panels.

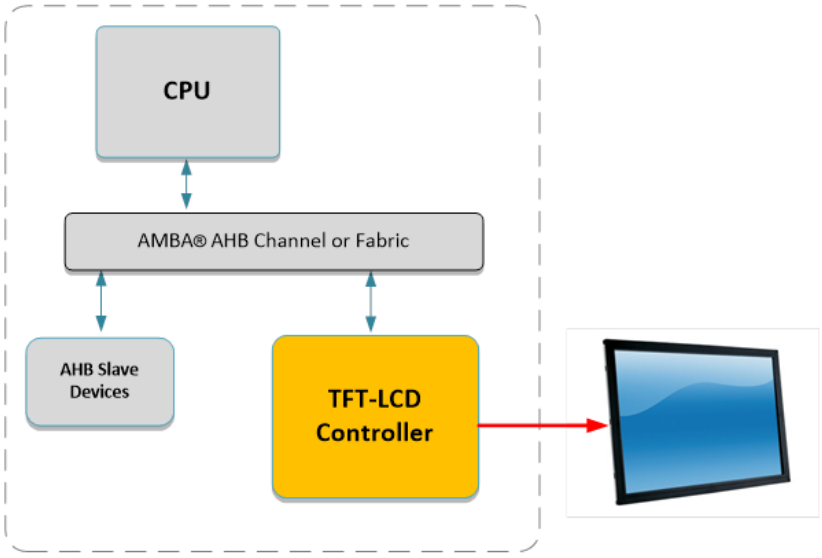
The AHB TFTLCD Controller supports 24-bit true color and 16-bit color, as well as an 8-bit color display mode via the 256 Pixel Palette Ram. A 24-bit true color multiplex mode is also supported in which 3 8-bit sub-pixels are time-multiplexed (R, G, B) on an 8-bit output. Pixel clock generation, Sync Control and Display Enable controls are fully programmable and can be used with a wide range of system clock rates.

The LCD data interface contains 8-bit Red, 8-bit Green, and 8-bit Blue for a total of 24bits. The LCD data interface will work with 6-bit RGB panels as well.

Interrupt sources timed to hsync, vsync and control signals are programmable and selectable to signal the processor to update display information.

The AHB TFTLCD supports an asynchronous clock input (lcdClk) as a timebase for pixel operations.

GENERAL USE



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You may also be interested in:

AMBA® Subsystems

- Low Power Subsystem (simple AHB system)
- Low Power / Performance Subsystem (includes AHB Multi-matrix Fabric)
- Custom Performance Subsystem (includes AXI Multi-layer Fabric)

IP Cores

Infrastructure Cores

AHB Multi-Matrix Fabric
AHB/AHBLite Channel
AHB Arbiter
AXI Multi-Layer Fabric
AXI to AHBLite Bridge
AXI to APB Bridge
AHB to ABP Bridge
APB Channel

AXI Cores

AXI Multi-Layer Fabric
AXI to AHBLite Bridge
AXI to APB Bridge
AXI External Bus Interface
(Memory/Flash Controller)
AXI Internal Memory Controller
AXI QSPI with Execute in Place (XIP)

AHB Cores

AHB Channel
AHB Multi-Matrix Fabric
AHB to ABP Bridge
AHB Arbiter
AHB QSPI with Execute in Place (XIP)
AHB External Bus Interface
AHB Internal SRAM Controller
AHB Interrupt Controller
AHB DMA Controller
AHB DMA 4 Channel Controller
AHB TFT LCD Controller
AHB DES/TDES Encryption/Decryption

AHB Serial Flash Controller
Octal, Quad, Dual and Single Modes

Serial to AHB Bridge
SPI slave to AHB Master
Monitor/Control

APB Cores

APB Channel
APB Quad SPI Controller
APB General Purpose IO
APB Timer
APB UART
APB I2C (Master and Slave)
APB SPI
APB Watchdog Timer
APB Pulse Width Modulator
APB Real Time Clock

General

DES – Digital Encryption Standard
Triple DES (Low Gates)
Triple DES (pipelined)
ADC Interface (semi-custom)
Mixed-Signal Interfaces (semi-custom)
Power Management Unit (semi-custom)

AES Encryption Core

For more information contact

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