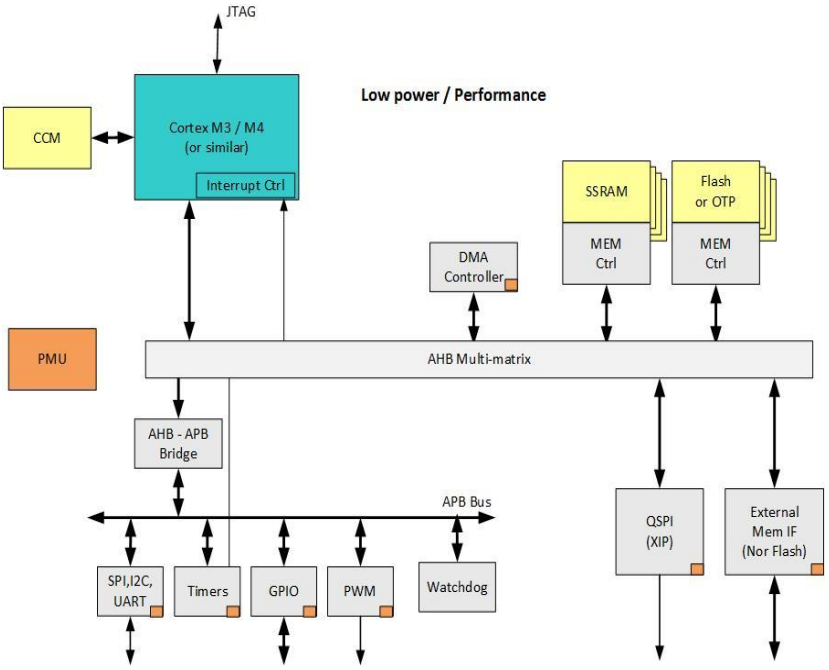
Low Power / Performance
Multi-matrix Subsystem

Features:

- Supports **Cortex-M3/M4** processors
- Power Management Unit
- AMBA® 2.0 (AHB)
- AHB Multi-matrix bus infrastructure
- External Nor Flash controller
- DMA (single or multi-channel)
- Internal SRAM controller
- Interrupt Controller (optional)
- QSPI with Execute in Place (XIP) for standard Flash parts such as Winbond and Spansion
- AHB/APB bridge
- Standard APB Peripheral package
  - I2C, SPI, UART, GPIO, Timers, Watchdog



Overview

The Low Power / Performance subsystem is a complete AMBA® 2.0 compliant Multi-matrix bus system. The subsystem is specifically designed for **Cortex®-M3** or **Cortex®-M4** based processor applications that target devices such as **industrial controllers**, **audio devices**, **motor control**, **wireless IoT** and **M2M** devices that need both low power and performance. Using **Cortex®-M3** or **Cortex®-M4** class processors give the subsystem the ability to perform DSP, spectral analysis or complex system control along with moving data efficiently using multiple DMA channels.

The QSPI core allows the subsystem to boot efficiently using standard external QSPI Flash memory from companies such as Winbond and Spansion. The QSPI Execute in Place (XIP) feature allows the subsystem to use smaller on-chip SRAM by the processor fetching instructions directly from off-chip Flash memory. This is especially efficient when using the Cortex-M3 or Cortex-M4 with L1 cache.

The subsystem also comes with a package of standard APB peripherals such as I2C, SPI, UART, Timer and Watchdog timer. All are supported with C-Code drivers and tests.

SoC Solutions LLC
49 Buford Highway
Suwanee, Georgia 30024
www.socsolutions.com

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Customization

The Low Power/Performance subsystem was designed to be easily customized. For example, we can optimize the number of channels in the Multi-matrix bus along with adding the proper number of DMA channels for the specific application's data movement needs.

The Power Management Unit is designed as two asynchronous power sequencing state-machines. The exact power sequences can be customized to best fit the application's power needs.

We use in-house integration tools to configure the APB subsystem to place the specific APB cores and number of instances you need.

Deliverables

The Low Power/Performance subsystem is delivered as Verilog Source, and includes everything required for successful implementation. The core is delivered with a complete subsystem-level test environment that is easily adaptable for additional integration.

AMBA® 2.0 Bus Functional Model is included for simulation and verification. Sample C driver and test code also included.

Integration and Verification Services

What better way to complete your design in the most efficient way than to use the engineers that created the basic system.

We offer integration and verification services to help you build your design around our subsystems. The SoC Solutions Team is experienced in Co-development using HDL(Verilog preferred) and custom software development.

Our services are flexible and customer-driven. We will work with you at any stage of the design process from architecture to implementation to system level verification to production readiness.

We ***jumpstart*** your design by providing boot-code, software, and interrupt service routines, for basic processor operation. Then we will work with you to successfully integrate your cores and expand the delivered subsystem test environment.

We can also help with the complete verification using C-code designed specifically for your application or test.

For more information contact

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