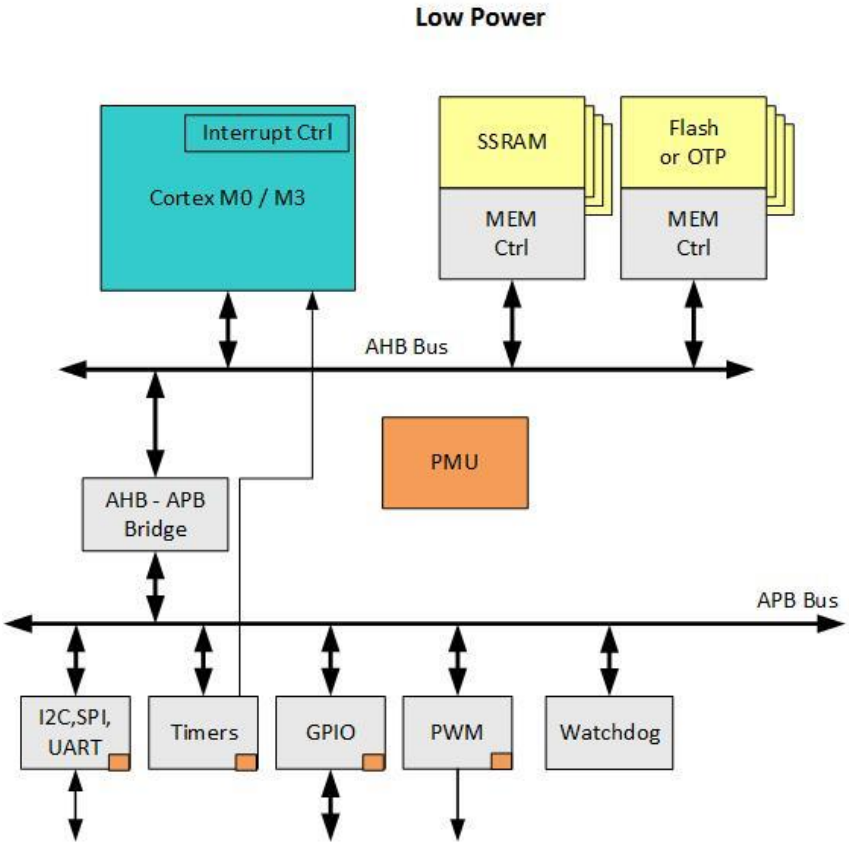
Low Power AHB
Subsystem

Features:

- Supports **Cortex-M0** (or equivalent) processors
- Power Management Unit
- AMBA® 3.0 (AHBLite) / APB bus infrastructure
- AHB/APB bridge
- Internal SRAM controller
- Interrupt Controller (optional)
- Standard APB Peripheral package
  - I2C, SPI, UART, GPIO, Timers, Watchdog



Overview

The Low Power subsystem is a complete AMBA® 3.0 compliant AHB/APB bus system. The subsystem is specifically designed for **Cortex®-M0** (or equivalent) based processor applications that target devices such as **water meter sensors**, **automobile sensors, implantable medical devices, IoT** and **M2M** devices that require ultra low power. Using a **Cortex®-M0** class processors gives the subsystem the ability to perform basic control while taking advantage of the low power management system minimize power, often from battery or energy harvesting sources.

The subsystem also comes with a package of standard APB peripherals such as I2C, SPI, UART, Timer and Watchdog timer. All are supported with C-Code drivers and tests.

SoC Solutions LLC
49 Buford Highway
Suwanee, Georgia 30024
www.socsolutions.com

Customization

The Low Power subsystem was designed to be easily customized.

The Power Management Unit is designed as two asynchronous power sequencing state-machines. The exact power sequences can be customized to best fit the application's power needs.

We use in-house integration tools to configure the APB subsystem to place the specific APB cores and number of instances you need.

Deliverables

The Low Power subsystem is delivered as Verilog Source, and includes everything required for successful implementation. The core is delivered with a complete subsystem-level test environment that is easily adaptable for additional integration.

AMBA® 2.0 Bus Functional Model is included for simulation and verification. Sample C driver and test code also included.

Integration and Verification Services

What better way to complete your design in the most efficient way than to use the engineers that created the basic system.

We offer integration and verification services to help you build your design around our subsystems. The SoC Solutions Team is experienced in Co-development using HDL(Verilog preferred) and custom software development.

Our services are flexible and customer-driven. We will work with you at any stage of the design process from architecture to implementation to system level verification to production readiness.

We ***jumpstart*** your design by providing boot-code, software, and interrupt service routines, for basic processor operation. Then we will work with you to successfully integrate your cores and expand the delivered subsystem test environment.

We can also help with the complete verification using C-code designed specifically for your application or test.

For more information contact

www.SoCSolutions.com

SoC Solutions LLC
49 Buford Highway
Suwanee, Georgia 30024
www.socsolutions.com